AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application:

1 - 20. (canceled)

21. (currently amended) A signal processing integrated circuit comprising at least one channel and each channel comprising ~~at least one~~ an input coupled to ~~a plurality of amplifiers~~ an amplifier, wherein the ~~amplifiers process at least one~~ amplifier processes an input signal coming to the ~~inputs~~ input, each channel further comprising:

~~at least one amplifier selected from said plurality of amplifiers~~ an output from said amplifier coupled to ~~at least one of the said inputs for processing said input signals and outputting the amplified signal~~ an input of a processing circuit;

~~a~~ wherein the processing circuit ~~for~~ further processes an ~~processing the said~~ amplified signal and ~~outputting the~~ outputs a processed signal,

a trigger circuit to produce at least one trigger signal using the said processed signal and output the said trigger signals, and

an output circuit system for outputting said processed

signals responsive to said input signals.

22. (previously presented) The integrated circuit of claim 21, wherein a polarity switching circuit is connected to said amplifiers.

23. (previously presented) The integrated circuit of claim 22, wherein said polarity switching circuit is externally controlled.

24 - 27. (canceled)

28. (previously presented) The integrated circuit of claim 21, further comprising a peak hold or sample and hold circuit coupled to output of at least one of said amplifiers.

29. (previously presented) The integrated circuit of claim 21, further comprising a plurality of comparators connected to said amplifiers.

30. (previously presented) The integrated circuit of claim 29, wherein the said comparators can be at least one of following types; leading edge, zero crossing, constant fraction comparators.

31. (previously presented) The integrated circuit of claim 29,

wherein said plurality of comparators enclose at least one pulse height range of the said input signals.

32. (previously presented) The integrated circuit of claim 30, further comprising a circuit coupled to at least one of said plurality of comparators, said circuit producing a fast trigger signal output.

33. (currently amended) The integrated circuit of claim 28, further comprising a circuit ~~to connect~~ connected to an output of said peak hold or sample and hold circuit is multiplexed to said output circuit system.

34. (previously presented) The integrated circuit of claim 29, wherein an output of at least one of said plurality of comparators initiates a readout cycle of said signal processing integrated circuit.

35 - 38. (canceled)

39. (currently amended) The integrated circuit of claim 21, wherein said output circuit system outputs a ~~readout~~ processed signal for one triggered channel of said plurality of integrated circuit channels and disables all remaining channels of said plurality of integrated circuit channels, wherein a time delay

between said readout signal and said disablement of said remaining channels is controlled by an externally supplied signal.

40 - 43. (canceled)

44. (previously presented) The integrated circuit of claim 29, further comprising a first comparator of said plurality of comparators is a low level discriminator, and

wherein at least one of said first comparator produces an output trigger when pulse height of the said processed input signal is larger than a first threshold voltage.

45. (previously presented) The integrated circuit of claim 29, further comprising a second comparator of said plurality of comparators wherein said second comparator is an upper level discriminator, and

wherein said second comparator only produces a signal when pulse height of the said processed input signal is larger than a second threshold voltage.

46. (currently amended) The integrated circuit of claim 21, further comprising ~~circuitry~~ a time difference measurement circuit connected to the output circuit system for measuring the arrival time difference of said input signals between different channels.

47. (canceled)

48. (previously presented) The integrated circuit of claim 29, wherein the plurality of comparators is a single comparator.

49. (previously presented) The integrated circuit of claim 29, wherein at least one of the plurality of comparators is a discriminator.

50. (previously presented) The integrated circuit of claim 29, wherein at least one of the plurality of comparators is a fast comparator.

51 - 52. (canceled)

53. (currently amended) The integrated circuit of claim 21, further comprising ~~circuitry for pole zero~~ a pole-zero circuit cancellation connected to the said amplifiers.

54 - 57. (canceled)

58. (previously presented) The integrated circuit of claim 46, further comprising circuitry for measuring time difference of said input signals between different channels by measuring the phase

difference of a Sine and Cosine wave simultaneously sent to each channel at the time when the said channel produces a trigger.